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PARALLEL OPERATION OF IGBTs

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Power MOSFETs parallel extremely well due to their positive temperature coefficient. The IGBT, being a combination of a power MOSFET and BJT, cannot be simply described as having either a negative or positive temperature coefficient. The temperature coefficient is dependent on the technology used in the IGBT's design; even within the same technology, it changes depending on the current density. Following a few simple guidelines will ensure success in your parallel IGBT designs.

The objectives of this *Design Tip* are to:

1. Discuss general considerations for paralleling IGBTs.
2. Discuss the effect of thermal coupling on current and temperature unbalance.
3. Discuss one method of device selection to achieve better sharing, and compare performance achieved for IR's 600V Fast IGBTs.
4. Compare performance achieved for IR's 600V UltraFast™ IGBTs.
5. Discuss multiple (> 2) parallel IGBT designs.

Background information on paralleling IGBTs is contained in Section VIII of Reference [1].

1. General Considerations

Paralleling semiconductors is not a trivial matter. Items that must be considered to successfully parallel IGBTs are: gate circuitry, layout considerations, current unbalance, and temperature unbalance between devices. Paralleling helps to reduce conduction losses and junction to case thermal resistance. However, switching losses remain the same, or may even increase. If they are the dominant losses, only a marginal improvement will be achieved by paralleling. Paralleling to take advantage of lower price of smaller devices should not be attempted without due consideration of the technical risks. Experimental results should be obtained at the extremes of the manufacturing tolerances.

The following is a list of suggestions to eliminate parasitic oscillation in *any* MOS-gated power transistor design:

1. Ensure the gate of the IGBT or MOSFET is looking into a stiff (voltage) source with as little impedance as practical. This advice applies equally well to both paralleled and single device designs.

2. Use at least 10Ω of gate isolation resistance on *each* device in parallel; locate the resistor physically close to the actual gate lead of the device.

3. Zener diodes in gate drive circuits may cause oscillations. Do not place them directly gate to emitter/source to control gate overvoltage, instead place them on the driver side of the gate isolation resistor(s), if required.

4. Capacitors in gate drive circuits may also cause oscillations. Do not place them directly gate to emitter/source to control switching times, instead increase the gate isolation resistor. Capacitors slow down switching, thereby increasing the switching unbalance between devices.

Layout Considerations

The importance of the physical circuit layout increases with both current and frequency. Significant effort should be made to keep stray inductance to an absolute minimum. A poor layout can contribute the following problems: voltage overshoot, poor switching performance, and poor conduction performance. The layout should be as tight, compact, and symmetrical as practical, and as the operating frequency and/or current increases, so should the distribution of capacitance used to decouple the stray circuit inductance. Of particular importance is the stray inductance in the loop of the gate drive return. This will cause the gate of the IGBT to see a different voltage than expected. Reference [2] and Reference [3] page 40 cover some of the problems that can be caused by poor layout or inadequate gate drive.

Unbalance Current vs. Temperature

When paralleling power semiconductors, the first issue that comes to mind is how well they share the total current. But, semiconductors are more sensitive to temperature than to current, so the real issue is how closely they are matched in junction temperature and whether or not one of the devices approaches the rated junction temperature. As junction temperature directly correlates to reliability, it should be of primary concern to the designer.

Current Unbalance

Given two different IGBTs, each $V_{CE(on)}$ for any given current level will be slightly different. When these two IGBTs are operated in parallel, the $V_{CE(on)}$ across both devices is forced to be the same. Thus, for a given load current, one IGBT will carry more current than the other, resulting in a current unbalance. *As long as the current remains below the maximum specified on the data sheet, current unbalance is not critically important.* At lower currents, it can be 75-100%.

Temperature Unbalance

Since the voltage drop is the same for both IGBTs, the device that carries more current has a higher junction temperature that may exceed the maximum rated junction temperature of 150°C. Combined with reliability issues, this factor should focus the designer's

primary concern on temperature unbalance.

2. Thermal Coupling and Other Balancing Factors

Thermal coupling is the key to reducing temperature unbalance. If the thermal coupling between the two devices is tight, the temperature differential cannot be significant. The other factor that reduces current unbalance is the temperature coefficient of the voltage drop. The IGBT with the lower voltage drop has a lower temperature coefficient. As current and temperature increase, its voltage drop changes little, while the voltage drop of the IGBT that was carrying little current comes down significantly, thereby closing the gap in current, as well as temperature.

The third balancing mechanism is due to one characteristic of the dynamic resistance of the devices. The IGBT with lower voltage drop has a higher dynamic resistance. This causes the two voltage drops to coverage at higher currents.

Current unbalance may not be affected significantly by thermal coupling. This is shown in the figures in the following section depicting current unbalance for IGBTs mounted on both separate and common heat sinks. However, the more important criteria, temperature unbalance, *is* affected significantly. In fact, the figures in the following section show that the maximum current is limited by the hotter device exceeding the 150°C maximum junction temperature rating. See Reference [1] Section VIII.B.3 for more information.

3. Device Selection for IR's 600V Fast IGBT

Device selection is an effective method to reduce derating that is intrinsically associated with paralleling and ensure that IGBTs are operated within data sheet limits. As a selection criteria, the voltage across each IGBT was measured at a certain current level. The configuration of this measurement is what we call "diode mode" (Figure 1) which means the gate is tied to the collector, and voltage is applied across that combined terminal and the emitter. The voltage is increased until the desired current is conducted through the IGBT. This measurement must be done in pulse mode to avoid device self-heating. The voltage required for this amount of current is recorded. This measurement not only takes into account variations in $V_{CE(on)}$, but also threshold, as well as g_{fs}. This "diode mode" voltage results in a convenient way to select IGBTs that will be paralleled. Matching only $V_{CE(on)}$ would be more appropriate for IGBTs not operated in switchmode. In the following two sections, simulations have been run on different pairs of IGBTs to compare temperature unbalance and current unbalance versus device variation measured using the "diode mode" voltage of the IGBT.

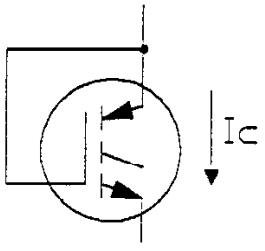

Figure 1 - Connection for Measuring "Diode Mode" Voltage, V_{diode}

Using this device selection strategy, we set out to devise a method of determining how well various pairs of IGBTs parallel in a typical half-bridge configuration. To this end, an empirical model was used for our IGBTs that models conduction and switching loss (see Reference [4]).

Five devices from each lot, using three lots, were examined and ranked in order of conduction voltage. Using this information, it is possible to obtain the operating point of IGBTs in parallel operation. To compare performance of various sets of IGBTs, graphs of percent current unbalance versus total current were developed. These graphs depict how much D.C. current unbalance can be expected for a given total current, for a particular pair of IGBTs. Two cases are plotted - devices mounted on separate heat sinks, and devices mounted on a common heat sink. Also generated were graphs of junction temperature of the higher of the two junctions versus total current. In these graphs, three curves are plotted: 1) perfectly matched devices with no unbalance, 2) devices unmatched by a value of ΔV_{diode} mounted on the same heat sink, and 3) devices unmatched by a value of ΔV_{diode} mounted on separate heat sinks.

Figure 2 depicts the percent current unbalance at different current levels for the two IRGPC50Fs at both ends of the spectrum: one has the lowest $V_{CE(on)}$, while the other has the highest $V_{CE(on)}$ of all the devices tested. The ΔV_{diode} for this pair of IGBTs was 0.69V. The operating conditions were: two devices mounted on either a common heat sink with an $R\theta_{SA}$ of 2°C/W, or separate heat sinks with $R\theta_{SA}$s of 4°C/W, with an ambient temperature of 45°C.

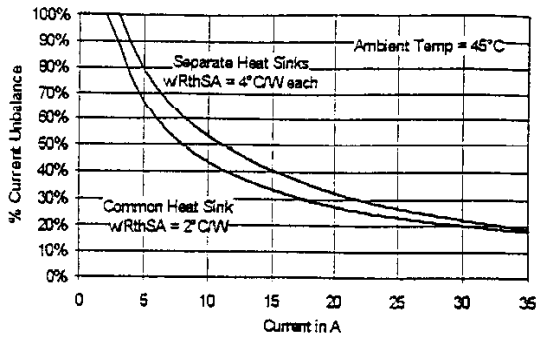

Figure 2 - Percent Current Unbalance versus Total Current. IRGPC50F with $\Delta V_{diode} = 0.69V$

As Figure 2 shows, at low currents, one IGBT carries all the current. As the current increases, the unbalance improves due to the three balancing mechanisms we mentioned above for the lower curve (same heat sink, therefore tight thermal coupling) and just the two related to current for the upper curve (separate heat sink).

Figure 3 depicts the higher junction temperature of the two IGBTs in parallel for three different cases: perfectly matched devices, the above two devices mounted on the same heat sink, and the above two devices mounted on different heat sinks. This figure provides the strongest argument for placing separate devices on the same heat sink: while conducting 20 A, the two worst case IGBTs' junction temperatures are within 2.5°C of the ideal case of perfectly matched IGBTs. However, the junction temperature of one of these same two devices mounted on separate heat sinks operates at an increased junction temperature of 16°C. Also note that the maximum allowable current is reduced from 35 A to 31 A. *All solely due to the devices' being mounted on separate heat sinks.*

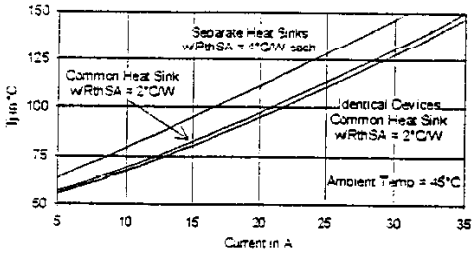

Figure 3 - Junction Temperature versus Total Current, IRGPC50F with ΔV_{diode} = 0.69V

The two devices in Figures 2 and 3 exhibited the largest range in V_{diode} of all 15 devices tested. The difference in V_{diode} voltages was 0.69 V measured at 20 A. For two devices that had a difference of 0.33 V at 20A, the graphs are shown in Figures 4 and 5.

These devices, mounted on separate heat sinks, are limited to a maximum current of 33 A, while devices on a common heat sink can operate to 35 A. While conducting 20 A, the two IGBTs' junction temperatures are within 1.5°C of the ideal case of perfectly matched IGBTs when mounted on a common heat sink. The same two devices mounted on separate heat sinks operate at an increased junction temperature of 8.3°C.

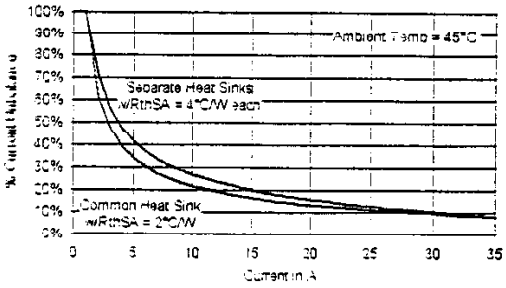

Figure 4 - Percent Current Unbalance versus Total Current, IRGPC50F with ΔV_{diode} = 0.33V

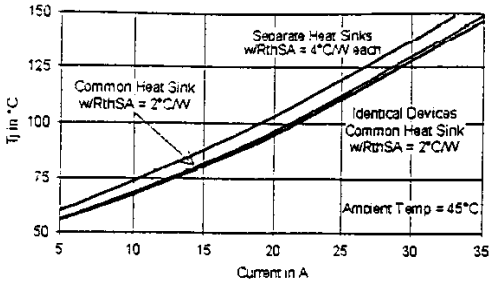

Figure 5 - Junction Temperature versus Total Current, IRGPC50F with ΔV_{diode} = 0.33V

The following two graphs depict the correlation of current unbalance and junction temperature versus V_{diode} measurements. *From these two figures, it is possible to predict the operation of a parallel pair of IGBTs given the difference in their "diode mode" voltages.* Figure 7 reinforces the importance of mounting the devices on the same heat sink.

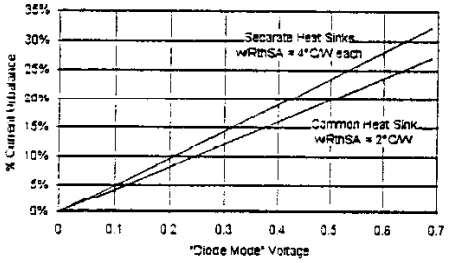

Figure 6 - Percent Current Unbalance versus ΔV_{diode}, IRGPC50F

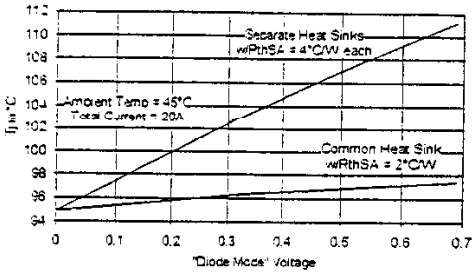

Figure 7 - Junction Temperature versus ΔV_{diode} IRGPC50F

Figure 8 depicts the reduction in output current in a half-bridge circuit due to junction temperature limitations between unmatched IGBTs. The circuit is operated under the same conditions as the previous ones, but instead of the current being fixed, the junction temperature is fixed at 125°C. Neither IGBT is allowed to exceed 125°C. The graph plots the maximum output current versus switching frequency. Notice that little or no derating is necessary under common applications or conditions.

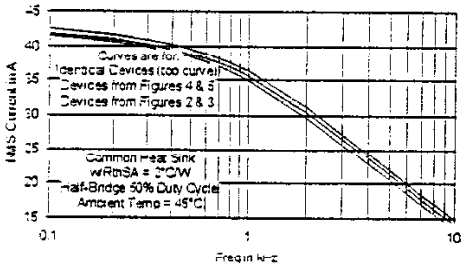

Figure 8 - Current versus Frequency Graph for Three Pairs of IRGPC50Fs with ΔV_{diode} = 0.00, 0.33, & 0.69V

The curves in Figure 8 were calculated assuming the two devices were mounted on a common heat sink. The case of separate heat sinks was not addressed due to concerns previously mentioned. The output current would be significantly reduced if the devices were on different heat sinks.

4. Device Selection for IR's 600V UltraFast™ IGBT

The method presented in the previous section was found to be inappropriate when the amount of lifetime killing (see Reference [5]) has a significant impact on the behavior of the device. For these devices, a simple $V_{CE(on)}$ matching scheme has been implemented. The following figures describe the performance achieved using various pairs of paralleled UltraFast IGBTs.

Figure 9 depicts the percent current unbalance at different current levels for the two IRGPC50Us at both ends of the spectrum: lowest and highest $V_{CE(on)}$s of the entire population of 15 devices from three lots. The $\Delta V_{CE(on)}$ for these was 0.55 volts measured at 30 amps. The operating conditions were: two devices mounted on a common heat sink with an $R\theta_{SA}$ of 2°C/W with an ambient temperature of 45°C.

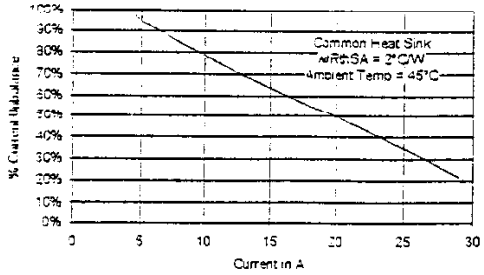

Figure 9 - Percent Current Unbalance versus Total Current, IRGPC50U with $\Delta V_{CE(on)}$ = 0.55V

While the current sharing displayed in Figure 9 may appear to be unacceptable, as discussed in the previous section, the more important factor is the junction temperature, which is shown in Figure 10. The upper curve in Figure 10 is for the devices in Figure 9, while the lower curve is for two identical (i.e., $\Delta V_{CE(on)}$

is zero). For any current, the penalty resulting from mismatched devices is only a few degrees Celsius.

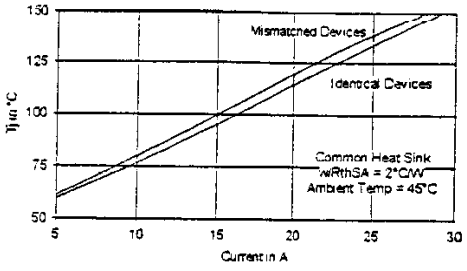

Figure 10 - Junction Temperature versus Total Current, IRGPC50U with $\Delta V_{CE(on)}$ = 0.55V

To compare closer matched devices, the above two figures were repeated using two devices with a $\Delta V_{CE(on)}$ = 0.36V measured at 30 amps. Figure 11 depicts the percent current unbalance at different current levels for two mismatched IRGPC50Us. The operating conditions are the same as the previous two figures.

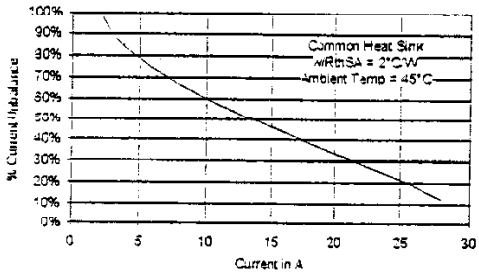

Figure 11 - Percent Current Unbalance versus Total Current, IRGPC50U with $\Delta V_{CE(on)}$ = 0.36V

Figure 12 depicts the junction temperature versus current. The upper curve in Figure 12 is for the devices in Figure 11, while the lower curve is for two identical (i.e., $\Delta V_{CE(on)}$ is zero).

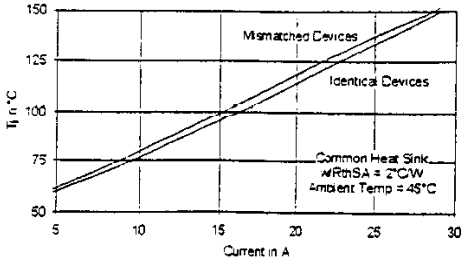

Figure 12 - Junction Temperature versus Total Current, IRGPC50U with $\Delta V_{CE(on)}$ = 0.36V

Figure 13 depicts the higher of the two junction temperatures for the parallel combination of several different pairs of IRGPC50Us with increasing $\Delta V_{CE(on)}$s. This graph describes why it is critically important that paralleled devices MUST be mounted on a common heat sink.

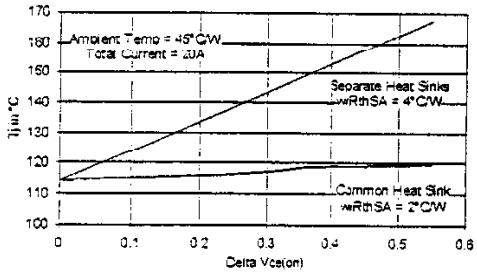

Figure 13 - Junction Temperature versus $\Delta V_{CE(on)}$ for IRGPC50Us

The final graph, Figure 14, depicts the RMS current versus switching frequency for a parallel pair of IRGPC50Us operated in a typical half-bridge configuration with 50% fixed duty cycle. The devices are mounted on a common heat sink with a thermal resistance of 2° C/W with an ambient temperature of 45° C. Neither IGBT is allowed to exceed a junction temperature of 125°C. The upper curve is for identical devices, the next curve is for the devices described in Figures 11 and 12, while the lower curve is for the devices described in Figures 9 and 10.

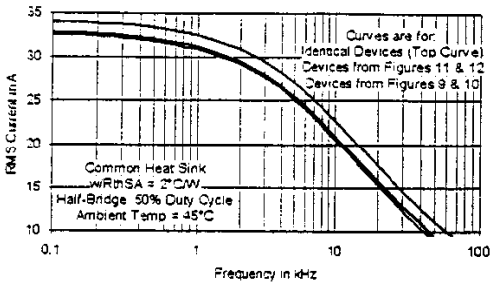

Figure 16 - Current versus Frequency Graph for Three Pairs of IRGPC50Us with ΔV_{dtode} = 0.00, 0.36, & 0.55V

As also shown in Figure 8 for the IRGPC50F devices, the output current of the half-bridge plotted in Figure 16 for two IRGPC50U devices is not significantly reduced due to the mismatch of $V_{CE(on)}$ between the two IGBTs, *if, and only if, they are mounted on a common heat sink which provides tight thermal coupling.*

5. Multiple Paralleled Devices

The previous discussions have been limited to two paralleled devices, the only case that can be treated with simple analytical tools. This does not limit the generality of the conclusions, however, as in any group of paralleled devices, there will be two with extreme voltage drops. As explained in Reference [1] Section VIII.B.1., these two are also likely to have extreme switching characteristics. The considerations of this Design Tip, specifically the selection criteria, would apply to these two extreme devices, with all others falling in between.

Conclusions

In paralleling IGBTs, precautions in layout, gate drive, and heat sinking are by far more important that current sharing. The critical parameter to be equalized is the junction temperature, as this directly correlates to the long term reliability of the devices. If the parallel IGBTs are mounted on the same heat sink, tight thermal feedback will be achieved. This feedback results in acceptable temperature unbalance in nearly all applications. Two methods of device selection targeted for switchmode operation are presented, but it are generally not necessary unless the IGBTs are being used near their maximum rating, i.e., with little or no derating.

References:

1. IR Application Note AN-990: *Application Characterization of IGBTs.*

2. James B. Forsythe, ***Paralleling of Power MOSFETs for Higher Power Output,*** PowerCon '81.

3. HEXFET Designer's Manual (HDM-1), 1992.

4. Clemente, S., Dapkus, D., ***Accurate Junction Temperature Calculation Optimizes IGBT Selection for Maximum Performance and Reliability.*** PCIM'92 Conference Proceedings.

5. IR Application Note AN-983A: *IGBT Characteristics.*