How to Design an R_g Resistor for a Vishay Trench PT IGBT

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INTRODUCTION

In low-switching-frequency applications like DC/AC stages for TIG welding equipment, the slow leg of a solar inverter, or a low-frequency converting structure where the maximum frequency is around 2 kHz, the IGBT has to guarantee the lowest possible conduction losses without switching losses affecting the device's overall efficiency. Historically, these requirements have been fulfilled using the well-consolidated planar Punch Through (PT) IGBT technology.

In response to an increasing demand for efficiency in the applications mentioned above, Vishay recently released a new technology approach that combines the benefits of a PT design with the advantages of a new MOS Trench structure. The overall electrical performances of the resulting PT Trench IGBT structure are further enhanced with an optimized lifetime killing technology.

Fig. 1 provides a comparison between a conventional planar PT IGBT unit cell with a planar MOS front-end and a Vishay PT Trench IGBT unit with a MOS cell made using the new technologies.

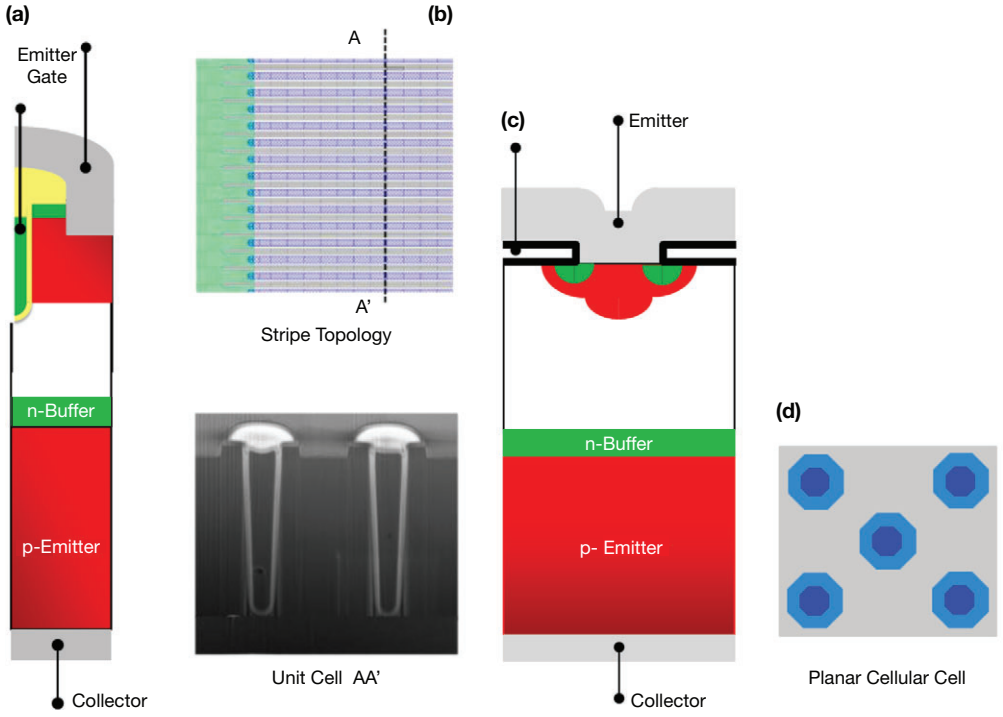

Fig. 1

PT Trench IGBT unit cell structure (a), cell topography, and cell cross section (b) compared with a planar PT unit cell structure (c) and cell topography (d).

APPLICATION NOTE

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Vishay's PT Trench IGBT technology achieves a significant improvement in overall performance by implementing these features:

- Faster turn-off capability due to the high hole confinement achieved by adopting the Trench MOS structure for the device's front-end. This design aspect allows for efficient hole accumulation close to the device's base junction, where the carrier has a quicker response during device turn-off.
- Lower $V_{CE(sat)}$ due to high cell density, an optimized doping profile, and lifetime killing technology.
- Device robustness due to an optimized doping profile and lifetime killing process.

PT Trench IGBT technology is capable of guaranteeing a maximum junction temperature of +150 °C, showing a temperature coefficient for the main electrical parameters that is comparable with planar IGBT technology. The MOS Trench structure of the device's front-end leads to different C_{ge}, C_{rss} capacitance, and dynamic behavior compared to planar devices, and these differences need to be taken into consideration when using a PT Trench IGBT.

CALCULATING THE GATE RESISTOR

The gate driver circuit is made from a driver with an internal resistance, the connection between the driver circuit and the power module (twisted wire or PCB), and the internal layout of the IGBT module (internal connection, wire bonding, or chip in parallel).

The connection between the driver and IGBT terminal is a second-order circuit because it has an inductance and the gate of the IGBT does not have a negligible capacitance. A simplified electric model of the circuit is show in Fig. 2.

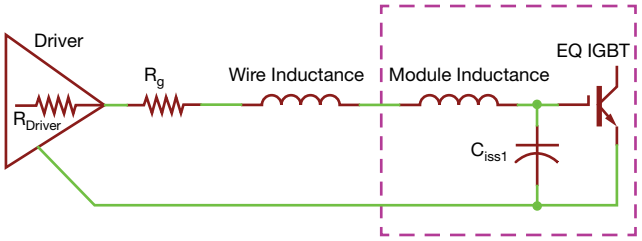

Fig. 2

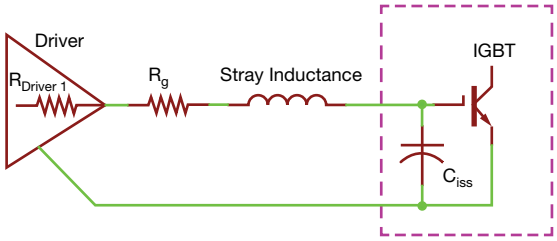

Fig. 3

The gate driver usually has low series resistance and negligible inductance if the output stage is a transistor output. If the output is a pulse transformer, the inductance must be evaluated and taken into account.

The connection between the gate driver and IGBT can be a wire or PCB, as show in Fig. 4. The inductance of wire connections varies by the type of cable, the number of twists per inch, diameter, length, etc. For PCB connections, stray inductance varies by the track layout.

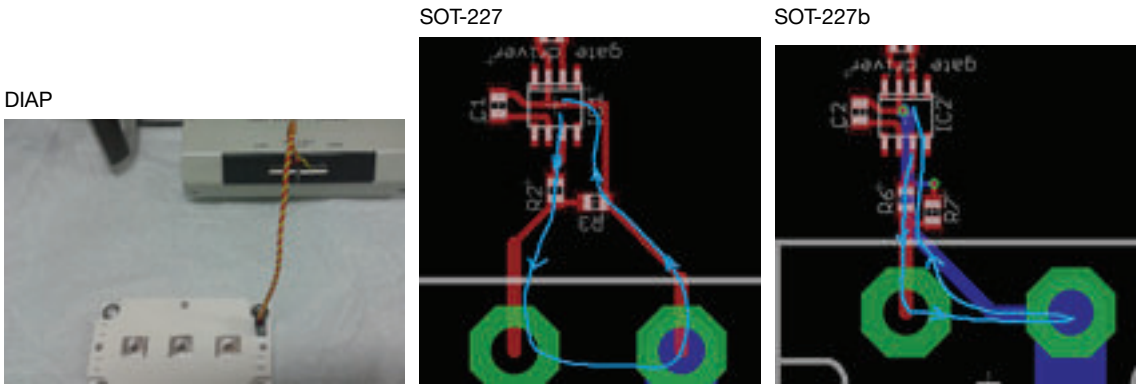

Fig. 4

In addition, at the external inductance there is internal inductance of the module due to the connection between the gate terminal and gate pad on the IGBT chip.

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The following table indicates the internal inductance of the modules where PT IGBT chips are mounted.

TABLE 1	
	L_S MODULE
GP250	12
GP100	30
GP300	87
GP400	114

This internal inductance is the equivalent of the inductance in-series at the gate-emitter connection, and is a function of the dimensions of the module.

The GP250 is a SOT-227 device with a very short gate-emitter connection and has a low inductance compared to the GP400, which is a larger DIAP module with several chips in parallel and a large gate connection.

To perform a practical evaluation of a gate circuit, consider a gate mesh circuit equivalent to that in Fig. 3, where it is possible to add up the values of the elements in series.

The V_{GE} voltage that switches the IGBT on and off is the voltage across a capacitor, C_{iss}, of the LC series circuit. This can be a problem because if the Q of the circuit is larger than 1, there will be oscillation on the V_{GE} that is not acceptable in certain cases. The Q of the circuit is a function of L_{stray}, C_{iss}, and R_g.

L_{stray} is related to the layout of the circuit, the driver, and the connection between the driver and IGBT.

The driver and gate connection has a very different inductance value, as a function of the layout, but it is a fixed value within the working conditions of the circuit.

The C_{iss} is the capacitance seen from the gate pin, which is the sum of internal capacitance C_{ge} and C_{gc}. This capacitance changes with the V_{GE}, V_{CE}, and temperature. Fig. 5 shows the behavior of the C_{iss}, C_{rss}, and C_{oss} as functions of the V_{CE}.

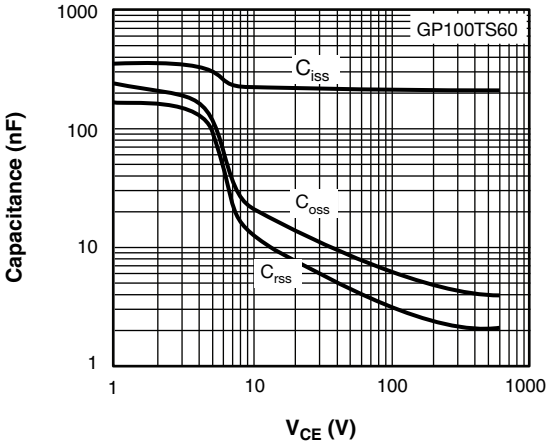

Fig. 5 - $C_{iss} = C_{ge} + C_{gc}$, $C_{rss} = C_{gc}$, $C_{oss} = C_{ce} + C_{gc}$

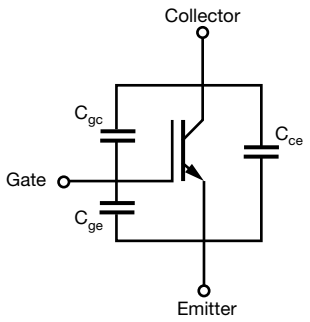

Fig. 6

Fig. 5 shows the capacitance of the GP100TS60, a large single-die device in the IAP. The capacitance varies with voltage and temperature, so evaluating the correct R_g value for the circuit in all conditions requires a field test.

A preliminary evaluation of R_g is possible, using the following formula, if there is an estimation of stray inductance:

$$R_g = 1.2\sqrt{\frac{L_{straymodule} + L_{gate\ cable}}{(C_{iss}\ \text{at}\ V_{CE} = 0\ V)}} \qquad (1)$$

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This value of R_g can be used as a first value for testing in the circuit. The final value can be fixed as a function of the different requirements in the circuit.

As an example we consider a circuit made with the GP100TS60. The module is connected to the driver with a twisted pair cable that is 25 cm long.

Fig. 7

The twisted pair cable (3 turn / cm) has a total inductance of 230 nH. The internal inductance of the module is 30 nH. The IGBT C_{iss} is 33 nF at V_{CE} = 0 V.

Using the formula (1) discussed above, we can determine that the R_g value is ≈ 3.3 Ω. This number is the initial value that can be used in a circuit for the preliminary test.

In a practical case the real inductance of the cable is only estimated or is unknown. The C_{iss} changes in respect to the operating conditions, so a field test is necessary to optimize the R_g, especially because R_g not only dumps the mesh gate but can control dI/dt and dV/dt - changing overshot and noise.

In the real circuit there are three common situations. The first is a large R_g with the gate signal behavior shown in Fig. 8. Here, the device is the GP100TS60 with R_g = 10 Ω and a 25 cm twisted pair cable. The C4 green track is the I_G, and the C1 blue track is the V_{GE} measured on the gate terminal as close as possible to the module. C2 cyan track V_{CE} is equal to 0 because only the effect of C_{ge} is considered.

This condition guarantees a smooth transition and that the voltage V_{GE} does not exceed the plateau limit. During turn-on the current flows only in a positive direction, and during turn-off it only flows in a negative direction.

The advantage of this kind of driving circuit is that the noise is very low, and a low current is required from the driver. The disadvantage is that E_{on} and E_{off} are not the minimum.

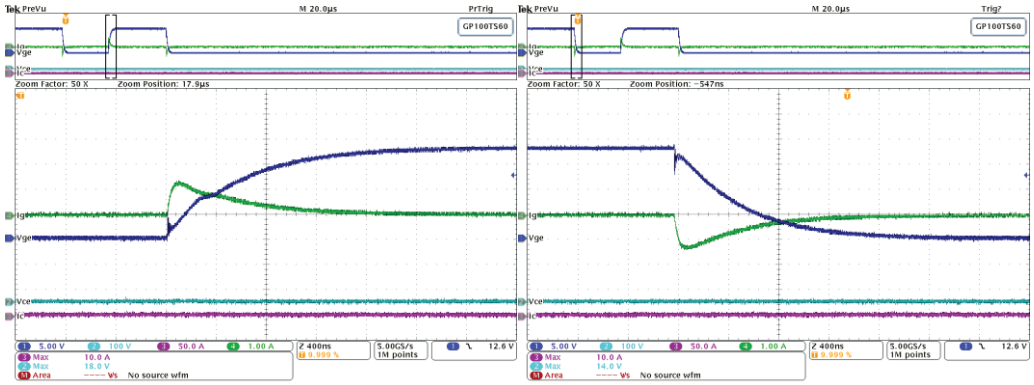

Fig. 8

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The second situation is a circuit with Q ≈ 1, as show in Fig. 9. Here, the device is the GP100TS60 with R_g = 3.4 Ω and 25 cm twisted pair cable. The C4 green track is the I_G, and the C1 blue track is the V_{GE} measured on the gate terminal as close as possible to the module. C2 V_{CE} is equal to 0 because only the effect of C_{ge} is considered.

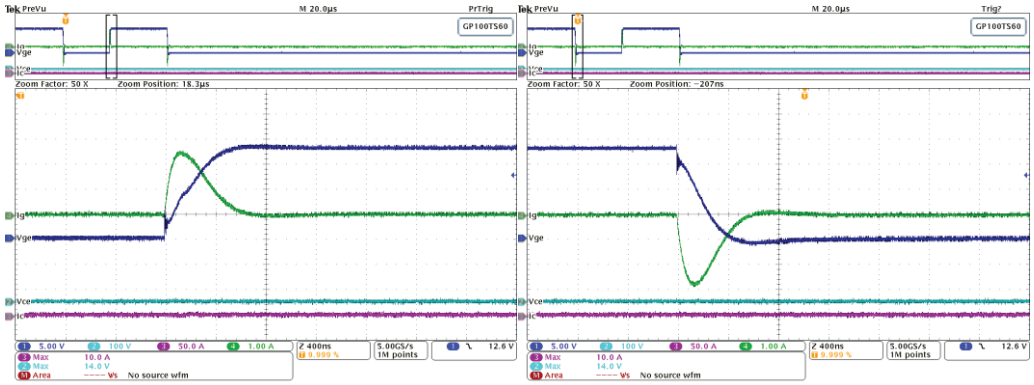

Fig. 9

This condition is the best compromise between noise and speed. The advantage of this kind of driving circuit is that E_{on} and E_{off} are at a minimum. The disadvantage is that more current is required from the driver.

In the third situation, the R_g gives a circuit with Q > 1, as show in Fig. 10. The device is the GP100TS60 with R_g = 1 Ω and 25 cm twisted pair cable. The C4 green track is the I_G, and the C1 blue track is the V_{GE} measured on the gate terminal as close as possible to the module. C2 V_{CE} is equal to 0 because only the effect of C_{ge} is considered.

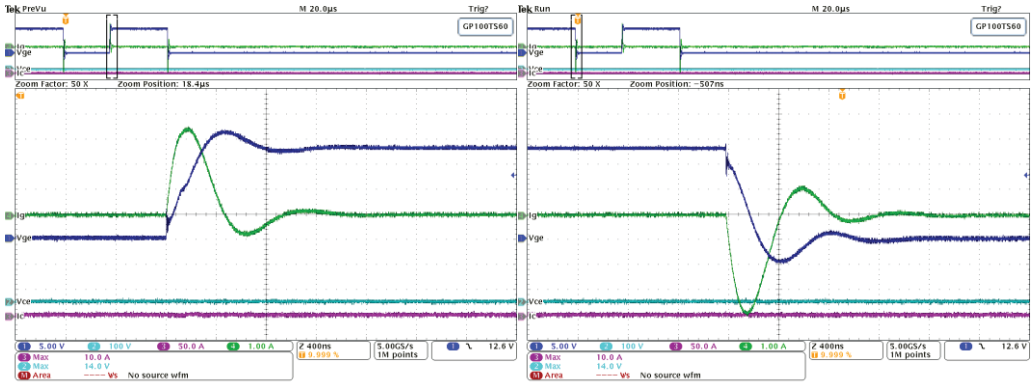

Fig. 10

There is a voltage overshoot that is tolerated from the device. The maximum voltage on the gate for an infinite time is limited to ± 20 V, but for a short time (< 1 µs) a voltage of ± 25 V can be applied. The V_{GE} voltage shows a ringing and I_G current flow during turn-on and turn-off times in the positive and negative directions.

This condition must be avoided because it does not provide lower switching losses, and if the secondary peak of V_{GE} oscillation becomes larger than the $V_{GE(th)}$, the IGBT can go into a linear zone during oscillation and the large dissipated energy can induce a failure due to high T_J.

In these three situations, the data matches well with the theory because the value of C_{iss} is quite constant and the RLC network model is good. If V_{CE} varies, however, the results are different. In the following three situations and figures, we use the same IGBT with the same R_g as before, but with a 400 V_{DC} bus and a switching inductive load.

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The first situation is a large R_g with gate signal behavior, as shown in Fig. 11. The device is the GP100TS60 with R_g = 10 Ω and 25 cm twisted pair cable. The C4 green track is the I_G, C1 blue track is the V_{GE}, C2 light blue is the V_{CE}, and C3 purple is the I_C.

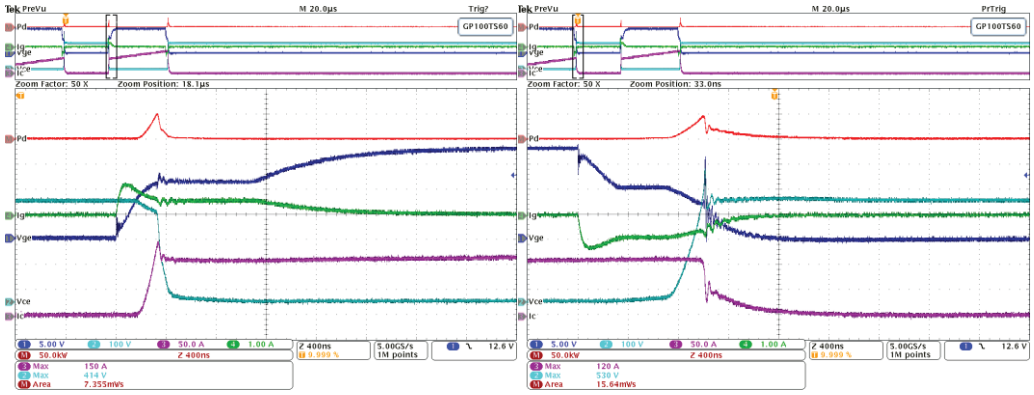

Fig. 11

This condition guarantees a smooth transition and that the V_{GE} does not exceed the positive and negative plateau limit. The I_{RRM} induced in the freewheeling diode is very low. The switching current is 120 A and the peak at the turn-on is 150 A, meaning that the I_{RRM} of the diode is only 30 A.

Now, with a large V_{CE}, there are evident effects due to the C_{rss} on the gate voltage. The Miller plateau in a high-voltage device is different from the effects that are usually expected in low-voltage devices like power MOSFETs.

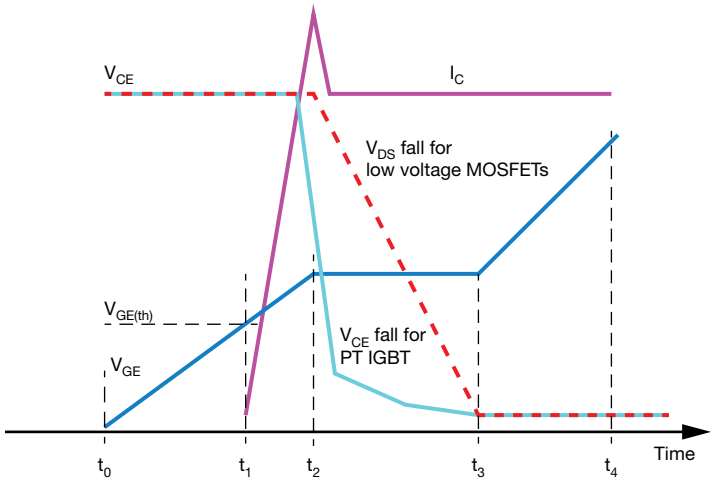

Fig. 12

Fig. 12 shows a comparison between a high-voltage Trench device and the behavior of a low-voltage MOSFET.

The behavior of V_{CE} is magnified to clarify the effect.

Soft V_{CE} voltage is normal during transition and it is almost invisible. It is less than 10 V to 15 V with time ≈ 400 ns and it is a normal behavior that is not usually due to poor driving. If V_{CE} show higher level and longer time the V_{GE} is usually poor and it has oscillation that is the signature of improper gate driving.

By applying the Miller theorem, a simple approximation of C_{iss} can be written as:

$$C_{iss}\,(V_{GE}, V_{CE}) = C_{ge}\,(V_{GE}) + C_{rss}\,(V_{CE})(1 + A_V\,(I_{CE}, V_{CE}, V_{GE})$$

In a low-voltage device there is a large A_V during the voltage transition. This is also true in a high-voltage device, but C_{rss} is small, so the maximum of the product $C_{rss}\,(V_{CE})$ 1 + $(A_V\,(I_{CE}, V_{CE}, V_{GE}))$ is when V_{CE} is around 20 V to 30 V.

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This effect changes the switching evolution. The real required Q_g is higher than the Q_g estimated from the capacitance. For this reason it is better use the Q_g data in the datasheet to evaluate the required power for the driver.

During the turn-off transition, it is possible to see two different slopes in the current I_C. In the first portion of current transition, the I_C drops quickly with a voltage overshoot. The peak arrives at 530 V; this is the MOSFET transition. The second portion is an exponential decay typical of bipolar recombination and does not produce any overshoot.

In the second situation, the R_g gives an input circuit with Q ≈ 1 as shown in Fig. 13. The device is the GP100TS60 with R_g = 3.4 Ω and a 25 cm twisted pair cable. The C4 green track is the I_G, C1 blue track is the V_{GE}, C2 light blue is the V_{CE}, and C3 purple is the I_C.

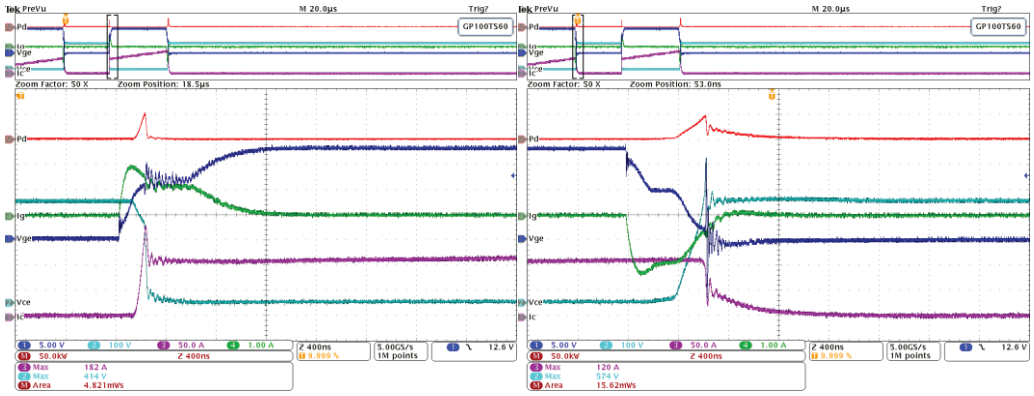

Fig. 13

Here, the I_G current does not show oscillation. During turn-on the current flow is only in a positive direction, and only in a negative direction during turn-off. This means that the V_{GE} is strictly increasing or strictly decreasing.

The IGBT stays in a linear zone only for the minimum time, the losses due to multiple transitions are avoided, and V_{CE} is as low as possible.

The I_{RRM} induced in the freewheeling diode in this configuration is higher. The switching current is 120 A and the peak at turn-on is 182 A. This means that the I_{RRM} of the diode is 62 A, but that the E_{on} losses are smaller because time is shorter. The peak of the I_G current is higher but the Q_g is similar, because the required charge for turn-on and turn-off is not strongly dependent on R_g.

Usually, the peak current in the driver is evaluated as

$$I_{G\,max.} = \frac{V_{CC} - (V_{EE} - V_{DR})}{R_g} \qquad (2)$$

Using this formula in this configuration with V_{CC} = 18 V, V_{EE} = 0 V, V_{DR} = 1 V (V_{CC} is the positive supply voltage of the driver, V_{EE} is the negative supply voltage of the driver, and V_{DR} is the voltage drop for the driver), and R_g = 3.4 Ω, the formula (2) gives a maximum I_G of 5 A. As is possible to see from Fig. 13, the I_G peak is -2.3 A. This is because the formula (2) considers only the resistive part of the gate mesh that is a very worst case scenario, like removing the module, or the wire from the driver, and closing the driver on a short circuit. This consideration leads to choosing an oversized driver that is not required for this kind of application.

Usually when the Q of an RLC network is ≈ 1, it is possible to choose a driver that has:

$$I_{G\,max.} = \frac{V_{CC} - (V_{EE} - V_{DR})}{2 \times R_g}$$

At the normal max. switching frequency of 1 kHz to 2 kHz, the required power is very low due to 2 x Q_g x f_{sw} being very low.

Also in this case, the behavior at turn-off shows a double slope. The first portion of current transition of the I_C drops quickly, inducing an overshoot peak that arrives at 570 V. The MOSFET transition and electric field recovery are heavily influenced by the R_g; with R_g = 10 Ω to R_g = 3.4 Ω, the overvoltage peak pass is from 530 V to 570 V. The second portion is an exponential decay of bipolar recombination that is quite independent from the R_g, so it does not change the behavior much.

The disadvantage here is that the voltage overshoot is higher, but that is not an issue for this device. Instead, it is the high dI/dt and dV/dt that can be a problem in terms of EMI. In regards to turn-off losses, the difference in E_{off} between devices that are

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driven with R_g = 10 Ω and R_g = 3.4 Ω is negligible; the reduction of R_g does not give a particular advantage in terms of switching losses. This explains how it is possible use a different R_g to change the dI/dt and dV/dt to solve the EMI problem without modifying the layout of the circuit.

If we consider turn-on, reducing the R_g decreases the E_{on} losses. For example, the GP100TS60 with an E_{on} of R_g = 10 Ω gives 7.3 mJ of losses for each commutation. Compared to an E_{on} of R_g = 3.4 Ω with 4.8 mJ of losses, the gain is huge.

If we think that a reasonable maximum switching frequency can be 2 kHz, the gain in terms of power is 5 W. For a device that handles 120 A, this is a small portion of the total losses.

In regards to turn-off, the E_{off} difference between a device that is driven with R_g = 10 Ω and R_g = 3.4 Ω is negligible; the same reduction in R_g does not give a particular advantage in terms of switching losses.

This explains how it is possible to use a different R_g to change the dI/dt and dV/dt to solve the EMI problem without modifying the layout.

In the third situation, the R_g provides a circuit with Q > 1, as show in Fig. 14. The device is the GP100TS60 with R_g = 1 Ω and a 25 cm twisted pair cable. The C4 green track is the I_G, C1 blue track is the V_{GE} measured on the gate terminal as close as possible to the module, C2 light blue is the V_{CE}, and C3 purple is the I_C.

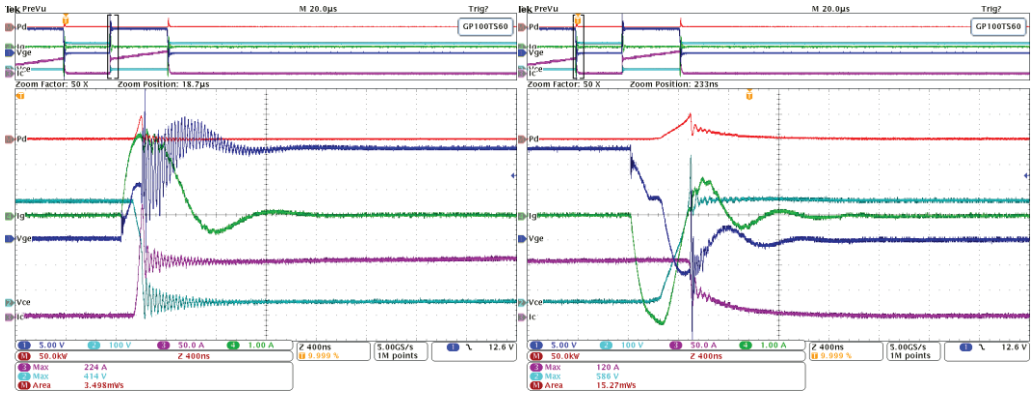

Fig. 14

The I_G current shows an oscillation during turn-on and turn-off, with the current flowing in a positive and negative direction. This behavior is reflected in an oscillation of the V_{GE}, which can be tolerated if the level of V_{GE} guarantees the state of the IGBT. Guaranteeing the state of the IGBT means that the V_{GE} voltage is high enough to assure a low V_{CE} when the IGBT is on, and low enough to assure a negligible I_C when the IGBT is off.

In Fig. 15, which it is an enlargement of the left side of Fig. 14, two kinds of oscillation are present. The first is due to ringing on the gate from too low R_g (compared with the V_{GE} voltage in Fig. 10), and the second is noise due to the ringing on V_{CE} produced by the quick recovery of the diode induced from the very high dI/dt.

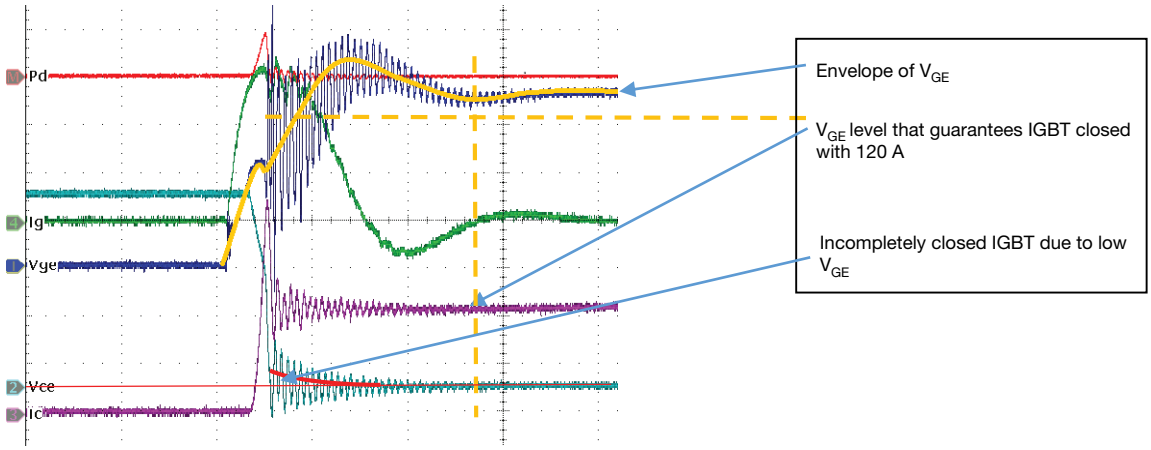

Fig. 15

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The high-frequency noise has a short period of < 25 ns, which is shorter than the t_d of the IGBT. For this reason, the modulation of conduction is negligible and the quick variation of V_{CE} is due to high-frequency current on the stray inductance of the module.

The average value of V_{CE}, which shows a sort of tail, demonstrates the low value of V_{GE} to carry 120 A. However, as is underlined in the instantaneous power (M-channel red track), the energy dissipated during this time is a small portion of the total energy.

There is a slow variation of V_{GE} after the turn-on change, but the value of V_{GE} does not go under the level that guarantees low V_{CE}. At the time indicated from the vertical slotted line, the local minimum is higher than 15 V.

If the oscillation of V_{GE} becomes greater, the IGBT could have a poor V_{CE}, which increases the losses that add to the E_{off}. For this reason, a suggested V_{GE} is around 18 V instead of the typical 15 V. 15 V is a good value, but must be guaranteed in any condition. If there is any doubt about the ability to guarantee 15 V in any condition, it is better to use a V_{GE} of 18 V or more. PT IGBT technology can work fine with V_{GE} near 20 V, and for a short time values of ± 25 V are safe.

Analyzing the turn-off in Fig. 14, we can see that oscillations on the current are longer and the Q of the circuit at turn-off is higher than at turn-on. This effect is due to the non-linear behavior of C_{iss} with the V_{CE}. For comparison, in Fig. 10 turn-on and turn-off are very similar because the V_{CE} is zero. Also in this case, it is possible to see two different kinds of oscillation. The lowest-frequency oscillation is related to the RLC circuit in the gate mesh. The quick oscillation in reality is noise due to the projection of V_{CE} on V_{GE} through the C_{rss}.

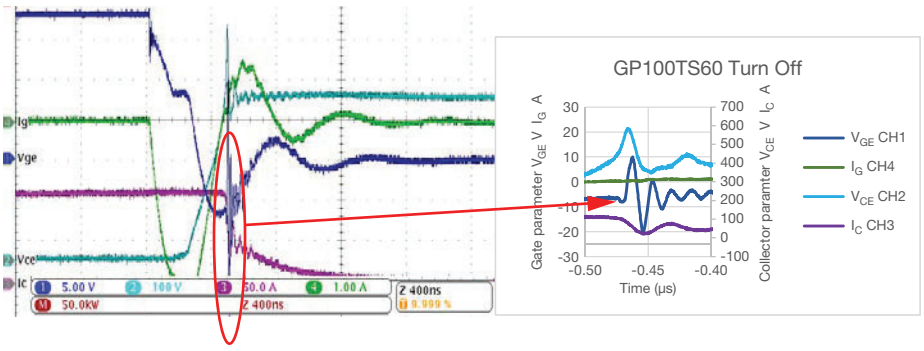

Fig. 16

In Fig. 16 there is an enlargement of Fig. 14. The slow oscillation carries the V_{GE} at a voltage lower than zero, which is not an issue but helps to switch off the MOSFET quickly, resulting in an overshoot of 580 V.

After the negative V_{GE} rise at a positive value, which can put the IGBT in conduction, a cross conduction of the IGBT leg with large dissipated energy can be produced.

To avoid this effect, it is usually better to drive the IGBT with a V_{GE} of negative value, but the PT Trench device does not require this feature on the driver in a normal condition. The real threshold voltage is high enough to guarantee a good margin and avoid cross conduction. This simplifies the design of the driver and avoids a negative voltage supply.

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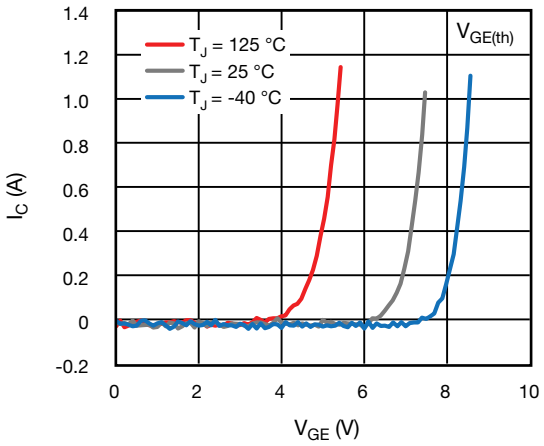

Fig. 17

An I_C around 1 A is not an issue for a short time (500 ns to 1000 ns) because the related energy is not too large. From this number with the data in Fig. 17, which shows the $V_{GE(th)}$ voltage, it is possible to evaluate the critical value of V_{GE}. For an I_C of 1 A at high temperature, the V_{GE} is around 5 V. If the V_{GE} ringing is lower than this value, the PT IGBT does not show a false turn-on or cross conduction problem. In Fig. 16, the maximum V_{GE} after commutation is around 3 V, which is a safe value.

At lower temperatures the margin is higher and the necessity for a negative V_{GE} is completely avoided. Note that in Fig. 17, the problem is not guaranteeing the off state at a low temperature, but having V_{GE} high enough to guarantee a low V_{CE} when the IGBT is in the on state after turn-on. For this reason as well, a V_{GE} larger than 15 V is often preferred.

In Fig. 16 there is a spike on V_{GE} voltage due to the quick variation on V_{CE}. During turn-off the gate mesh must be extended at C_{rss} because the current from the C_{rss} capacitor could be comparable with the current from the driver.

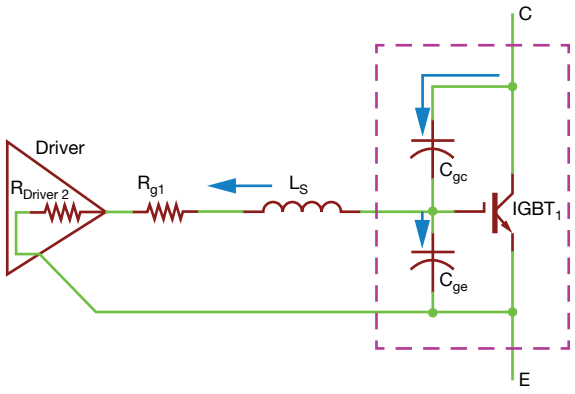

Fig. 18

Fig. 18 shows a simplified circuit of an IGBT during turn-off. When V_{CE} increases, the C_{gc} capacitor requires a current that flows in the gate node, increasing the V_{GE} because the current drained from the driver is $I_{RG1} \approx \frac{V_{GE} - V_{DR}}{2(R_{g1} + R_{Driver})}$ and the current that arrives from the C_{gc} is $I_{Cgc} \approx C_{gc}\ (V_{CE})\frac{dV_{CE}}{dt}$. V_{GE} is usually negligible compared with V_{CE}, so $V_{CG} \approx V_{CE}$.

At a high V_{CE}, the C_{rss} is small but $\frac{dV_{CE}}{dt}$ is very high. The current I_{Rg1} during this transient is quite constant, because it is forced from the inductance L_S. So the value of V_{GE} is defined by the ratio between C_{gc} and C_{ge}.

APPLICATION NOTE

How to Design an R_g Resistor for a Vishay Trench PT IGBT

Reducing the R_g can help to keep control of the V_{GE}, but reducing R_g could produce oscillation due to the high Q factor of the R_{LC} circuit. One simple solution if the connection between the driver and IGBT is long and has large inductance is to place a small capacitor in parallel at the gate.

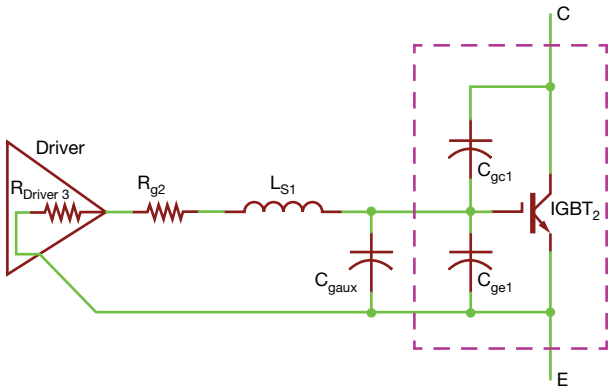

Fig. 19

Fig. 19 shows the gate circuit with the auxiliary capacitor C_{gaux}, which must be mounted near the module or any inductance between the gate connection and the capacitor reduces its effect. The initial value of C_{gaux} can be equal to the value of C_{iss} at V_{CE} without overshoot (substantially the DC bus value) or 15 % of C_{iss} at V_{CE} = 0 V. The R_g must be revised with the same procedure at the formula (1), with the difference being that C_{iss} is now:

$$C_{iss} + (C_{gaux} \times R_g) = 1.2 \sqrt{\frac{L_{straymodule} + L_{gate\ cable}}{C_{iss}\ \text{at}\ V_{CE} = 0\ V + C_{gaux}}} \qquad (3)$$

APPLICATION NOTE

How to Design an R_g Resistor for a Vishay Trench PT IGBT

CONCLUSION

The optimum R_g value for an application must take into account the working conditions and the trade off between efficiency and noise. In any case, the third condition presented in this application note must be avoided, and a signal with behavior similar to the V_{GE} in Fig. 9 will give the best compromise between noise and switching losses. The third condition could reduce switching losses, but in a situation where switching losses are the small portion of global losses, the advantages in term of efficiency are negligible.

If there is noise induced from too high dV/dt or dI/dt, it is possible to control it with R_g.

The behavior of the IGBT during switching can be changed by choosing the right value of R_g and dV/dt across the CE terminal. If the R_g required is too large and the dV_{CE}/dt injects noise at the gate, a small capacitor can be placed in parallel near the gate terminal. Usually $V_{CE(t)}$ changes with the R_g of an IGBT, but if the IGBT works in a circuit with soft switching, it is possible to control dI/dt and dV/dt independently from the R_g.

In general, there is feedback from the collector to the emitter between the C_{gc} that changes the real V_{GE} across the gate of the IGBT. In this case, there are not general rules. Any circuit requires the appropriate value of R_g based on the required characteristic.

The behavior of the IGBT during turn-on and turn-off can be controlled through the R_g. The V_{CE} overshoot can be controlled with $R_{g\ off}$, while the peak of I_{RRM} in the diode can be controlled with $R_{g\ on}$. Many other parameters are influenced by R_g, as shown in Table 2.

TABLE 2

RATING / CHARACTERISTICS	R_g ↗	R_g ↘
$t_{d(on)}$	↗	↘
$t_{d(off)}$	↗	↘
E_{on}	↗	↘
E_{off}	↗	↘
E_{rec}	↘	↗
Turn on I_{pk}	↘	↗
Diode I_{RRM}	↘	↗
dV/dt	↘	↗
dI/dt	↘	↗
Voltage overshot	↘	↗
EMI noise	↘	↗

The target of a good design is to obtain the highest efficiency but also have the right margin in terms of V_{CE} and to respect EMI limits.